



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,531	09/30/2003	Dinh Quoc Nguyen	100-23200 (P05700)	8327

33402 7590 03/19/2004

LAW OFFICES OF MARK C. PICKERING
P.O. BOX 300
PETALUMA, CA 94953

EXAMINER

FENTY, JESSE A

ART UNIT	PAPER NUMBER
----------	--------------

2815

DATE MAILED: 03/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/676,531	Applicant(s) NGUYEN, DINH QUOC	
	Examiner Jesse A. Fenty	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 16-19 is/are rejected.
- 7) ☒ Claim(s) 7-15 and 20 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>093003</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6 and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Ker et al. (U.S. Patent No. 5,959,820).

In re claim 1, Ker (Fig. 5C) discloses a semiconductor device, comprising:

A semiconductor material (P-substrate) of a first conductivity type having a top surface and a dopant concentration;

A first well (left N-well of PCLSCR 2) of a second conductivity type formed in the semiconductor material, the first well contacting the top surface of the semiconductor material and having a dopant concentration;

A first semiconductor region (P+ in middle) of the first conductivity type formed in the first well, the first semiconductor region having a greater dopant concentration than the dopant concentration of the semiconductor material; and

A second semiconductor region (N+) of the second conductivity type formed in the first well, the second semiconductor region having a greater dopant concentration than the dopant concentration of the first well.

In re claim 2, Ker discloses the device of claim 1, further comprising:

Art Unit: 2815

A third semiconductor material region (P+ on right) of the first conductivity type formed in the semiconductor material, the third semiconductor region contacting the first well and the semiconductor material, being spaced apart from the first and second semiconductor regions, and having a greater dopant concentration than the dopant concentration of the semiconductor material.

In re claim 3, Ker discloses the device of claim 2, further comprising:

A second well (left N-well of PCLSCR n) of the second conductivity type formed in the semiconductor material, the second well contacting the top surface of the semiconductor material, and being space apart from the first well; and

A fourth semiconductor region (P+ on right) of the first conductivity type formed in the semiconductor material, the fourth semiconductor region contacting the top surface of the semiconductor material, the second well, and the semiconductor material, and having a greater dopant concentration than the dopant concentration of the semiconductor material.

In re claim 4, Ker discloses the device of claim 3, further comprising:

A fifth semiconductor region (P+ in middle) of the first conductivity type formed in the second well, the fifth semiconductor region contacting the top surface of the semiconductor material, being spaced apart from the fourth semiconductor region, and having a greater dopant concentration than the dopant concentration of the second well.

In re claim 5, Ker discloses the device of claim 4, further comprising a sixth semiconductor region (N+) of the second conductivity type formed in the second well, the sixth semiconductor region contacting the top surface of the semiconductor material, being spaced

Art Unit: 2815

apart from the fourth semiconductor region, and having a greater dopant concentration than the dopant concentration of the second well.

In re claim 6, Ker discloses the device of claim 5, wherein the fifth semiconductor region is spaced apart from a junction between the second well and the semiconductor material; and the sixth semiconductor region is spaced apart from the junction between the second well and the semiconductor material.

In re claim 16, Ker (Fig. 5C) discloses a method of making a semiconductor device having:

A semiconductor material (P-Substrate) of a first conductivity type, the semiconductor material having a top surface, the method comprising the steps of:

Forming a first well (left N-well of PCLSCR 2) and a second well (left N-well of PCLSCR n) of a second conductivity type in the semiconductor material;

Forming a plurality of regions (P+) of the first conductivity type in the top surface of the semiconductor material so that a first semiconductor region lies in the first well and a second semiconductor region lies in the second well; and

Forming a plurality of regions (N+) of the second conductivity type in the top surface of the semiconductor material so that a third semiconductor region lies in the first well and a fourth semiconductor region lies in the second well.

In re claim 17, Ker discloses the method of claim 16, wherein the plurality of regions of the first conductivity type include a fifth semiconductor region (P+) that contacts the first well and the semiconductor material, and is spaced apart from the first and third semiconductor regions.

Art Unit: 2815

In re claim 18, Ker discloses the method of claim 17, wherein the plurality of regions of the first conductivity type include a sixth semiconductor region (P+) that contacts the second well and the semiconductor material, and is spaced apart from the second and fourth semiconductor regions.

In re claim 19, Ker discloses the method of claim 17, wherein:

The first and third semiconductor regions are spaced apart from a junction between the first well and the semiconductor material; and

The second and fourth semiconductor regions are spaced apart from a junction between the second well and the semiconductor material.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Cheng et al. (US 2003/0038298 A1).

In re claim 1, Cheng (Fig. 6) discloses a semiconductor device, comprising:

A semiconductor material (21) of a first conductivity type having a top surface and a dopant concentration;

A first well (N-well on left side of the device) of a second conductivity type formed in the semiconductor material, the first well contacting the top surface of the semiconductor material and having a dopant concentration;

Art Unit: 2815

A first semiconductor region (P+) of the first conductivity type formed in the first well, the first semiconductor region having a greater dopant concentration than the dopant concentration of the semiconductor material; and

A second semiconductor region (N+) of the second conductivity type formed in the first well, the second semiconductor region having a greater dopant concentration than the dopant concentration of the first well.

In re claim 16, Cheng (Figs. 6, 9) discloses a method of making a semiconductor device having:

A semiconductor material (21) of a first conductivity type, the semiconductor material having a top surface, the method comprising the steps of:

Forming a first well (N-well on the left side of the device) and a second well (N-well on the right side of the device) of a second conductivity type in the semiconductor material;

Forming a plurality of regions (P+) of the first conductivity type in the top surface of the semiconductor material so that a first semiconductor region lies in the first well and a second semiconductor region lies in the second well; and

Forming a plurality of regions (N+) of the second conductivity type in the top surface of the semiconductor material so that a third semiconductor region lies in the first well and a fourth semiconductor region lies in the second well.

4. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Lai et al. (US 2003/0234405 A1).

In re claim 1, Lai (Figs. 5, 6) discloses a semiconductor device, comprising:

Art Unit: 2815

A semiconductor material (400) of a first conductivity type (P; section [0026], lines 7-8) having a top surface and a dopant concentration;

A first well (412) of a second conductivity type formed in the semiconductor material, the first well contacting the top surface of the semiconductor material and having a dopant concentration;

A first semiconductor region (432) of the first conductivity type formed in the first well, the first semiconductor region having a greater dopant concentration than the dopant concentration of the semiconductor material; and

A second semiconductor region (430) of the second conductivity type formed in the first well, the second semiconductor region having a greater dopant concentration than the dopant concentration of the first well.

In re claim 2, Lai discloses the device of claim 1, further comprising:

A third semiconductor material region (440) of the first conductivity type formed in the semiconductor material, the third semiconductor region contacting the first well and the semiconductor material, being spaced apart from the first and second semiconductor regions, and having a greater dopant concentration than the dopant concentration of the semiconductor material.

Allowable Subject Matter

5. Claims 7-15 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

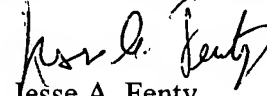
Art Unit: 2815

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Jesse A. Fenty
Examiner
Art Unit 2815